Course Title:	*Digital Logic Design*
Course Code:	CEN 120
Credit Hours Theory:	Three (3)
Credit Hours Lab (If Applicable):	0
Instructor Name with Qualification:	Bilal Ashraf Awan, MS, BE
Course Objectives:	This course will provide an introduction to the fundamental concepts and techniques underlying the construction of digital systems
Course Learning Outcomes:	**Professional and reflective practitioner skills** 1. Students learn how to analyze digital logic circuits. 2. Students learn how to design digital logic circuits. 3. Students learn to write and interpret documentation for digital systems. **Practical skills** 4. Students learn to implement and test digital circuits using SSI, MSI logic elements in lab environment. **Cognitive skills** 5. Students should be able understand the design principles and techniques used for Arithmetic and logic unit of computer
Contents (Catalog Description):	This course covers design of digital systems using standard, small, and medium scale integrated circuits. The main emphasis is on the theoretical concepts and systematic synthesis techniques that can be applied to the design of practical digital systems.
Recommended Text Books:	• Mano, M Morris; Digital Design 4th Ed
Reference Books:	• Digital Systems; Principles and Applications. Tocci, Widmer & Moss. 10th Edition • Digital Design 3rd Edition, Morris Mano • Jain, R.P.; Logic Design Digital Principles, 3rd Ed, Roger L Tokheim; Shaum's Outlines Series

Helping Web Sites:

http://dspace.mit.edu/handle/1721.1/49431

http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-004-computation-structures-spring-2009/

General Instructions for students:

Home Works and Assignments

Attendance is mandatory. Every class is important. All deadlines are hard. Under normal circumstances late work will not be accepted. Students are required to take all the tests. No make-up tests will be given under normal circumstances. Any form of cheating on exams/assignments/quizzes is subject to serious penalty

Attendance

75% attendance is mandatory. Latecomers will be marked as absent.

Evaluation Criteria

Assignments/projects	20%
Quizzes	10%
Mid-Term	20%
Final	50%

Quizzes Schedule

Quiz # 1	Week # 4
Quiz # 2	Week # 7
Quiz # 3	Week # 11
Quiz # 4	Week # 14

Assignments Schedule

Assignment	Delivery date	Submission Date
Assignment # 1	Week # 2	Week # 4
Assignment # 2	Week # 5	Week # 6
Assignment # 3	Week # 9	Week # 10
Assignment # 4	Week #11	Week #12

Sixteen Week Lesson Plan

Week #	Topic Planned
1	Introduction, course layout, analog vs discrete logic. Numbers Systems. Binary, Octa, Dec, Hex numbers and Conversions
2	1's and 2's complement. Subtraction using 2's complement Signed Number representation BCD Code, 2421 Code, Excess-3 code, Gray Code, ASCII.

3	Boolean Logic. TTL input/output voltage levels. Ch02: Review; Boolean algebra, Boolean postulates & theorems. Expression of Digital Function in Boolean Algebra. Canonical Forms; Sum of minterms, Product of maxterms. Standard Forms: SOP, POS. Conversion between forms. Positive and Negative Logic.
4	Ch03. Gate Level Minimization. K-map 2 variable, 3 variable, 4 variable, 5 variable Prime Implicants (PI), Essential prime Implicants (EPI). Don't Care conditions.
5	Two level NAND implementation. Problems. Multi level NAND implementation. Pr 3.18, 3.20. NOR implementation. Two level. Exclusive OR, Parity Generator/checker Multilevel
6	NOR implementation. Ch04: Combinational Circuits, Design. Analysis. Example. BCD to Excess-3 Converter
7	Half Adder, Full Adder. 4 bit Binary Adder. BCD Adder.
8	Combinational circuit building blocks. Decoder / *demultiplexer* synthesis of logic functions using decoders multiplexer / demultiplexer. Function implementation using multiplexers
9	Midterm
10	Ch05: Sequential Circuits. Introduction. Latches: SR, S'R', D Latch. Edge Triggering. Negative Edge triggered D Flip-flop Positive-Edge triggered D Flip-flop JK Flip Flop, T Flip Flop: Characteristic Table, characteristic equations
11	Analysis of Clocked Sequential Circuits. State Equation, State Table, State Diagram using D-Flip-Flop Analysis with JK Flip Flop. Examples. Analysis with T Flip Flop. Examples.
12	State Reduction and Assignments. Design of clocked Sequential Circuits. Design with D Flip Flop.

13	Design with JK Flip Flop. Design with T Flip Flop. Examples.
14	Design with Flip Flops. Problems. Ch 06: Registers. 4-bit registers. Shift registers. Serial addition.
15	Universal Shift Register Ripple Counters: Binary ripple counter. BCD Ripple counter. Synchronous counters: Binary counter, Up Down binary counter.
16	BCD counter. Binary counter with Parallel load. Ring Counters, Johnson Counter. Problems. Project Viva and Presentations.
17	Revision Week.
18	Finals Week

Course Learning Outcomes mapping to Program Learning Objectives

CONTRIBUTION OF COURSE LEARNING OUTCOMES TO PROGRAMME LEARNING OUTCOMES													
SOFTWARE ENGINEERING		**DIGITAL LOGIC DESIGN**											
No.	**Program Outcomes**	**Course Learning Outcomes**											
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
1	Engineering Knowledge			✓									
2	Problem analysis			✓									
3	Design/Development of solutions			✓									
4	Investigation												
5	Modern tool usage				✓								
6	Engineer and society												
7	Environment and sustainability												
8	Ethics												
9	Individual and Team work			✓									
10	Communication												
11	Project Management												
12	Lifelong learning												